

In the claims:

Cancel claim 1 and replace with claim 9 and amend as follows:

1. Cancelled
2. Cancelled
3. (three times amended) The non-volatile memory cell of claim [1] 9 wherein said ~~small spacer resides~~ connecting conductive layer extends along a side of the small sidewall spacer and on top of said main floating gate region.
4. (currently amended) The non-volatile memory cell of claim [3] 9 wherein said first insulating portion is over said drain.
5. (original) The non-volatile memory cell of claim 4 wherein said drain and source are self-aligned with the opposing sides of said main floating gate region.
6. (currently amended) The non-volatile memory cell of claim [1] 9 wherein said ~~small sidewall spacer resides~~ connecting conductive layer extends along a side ~~and on top~~ of said main floating gate region, the thin tunnel oxide insulation having a portion covering the main floating gate region except for an opening therein, with the connecting conductive layer making contact with the main floating gate region through said opening.
7. (currently amended) The non-volatile memory cell of claim [1] 4 wherein said first insulating portion ~~is over said drain~~ extends continuously across the memory cell.

8. (currently amended) The non-volatile memory cell of claim [1] 5 wherein said drain and source ~~are self-aligned with the opposing sides of said main floating gate region~~ each have a polysilicon spacer thereover.

9. (new) A non-volatile memory cell comprising:

a semiconductor substrate, with a drain and a source in the substrate;

a conductive floating gate formed on the substrate between the source and drain with a first insulating layer separating said floating gate from said substrate, said floating gate including a main floating gate region and a small sidewall spacer, said first insulating layer including a first insulating portion separating said small sidewall spacer from the substrate and from the main floating gate region, said second insulating portion separating said main floating gate region from said substrate, wherein the first insulating portion is thin tunnel oxide that is thinner than said second insulating portion, said small sidewall spacer having a first side contacting the thin tunnel oxide insulation and an opposite side that is electrically coupled to the main floating gate region by a conductive connecting layer extending over said opposite side of the sidewall spacer and extending past the thin tunnel oxide to contact the main floating gate region;

a control gate formed over the floating gate; and

a second insulating layer separating said control gate and said floating gate.